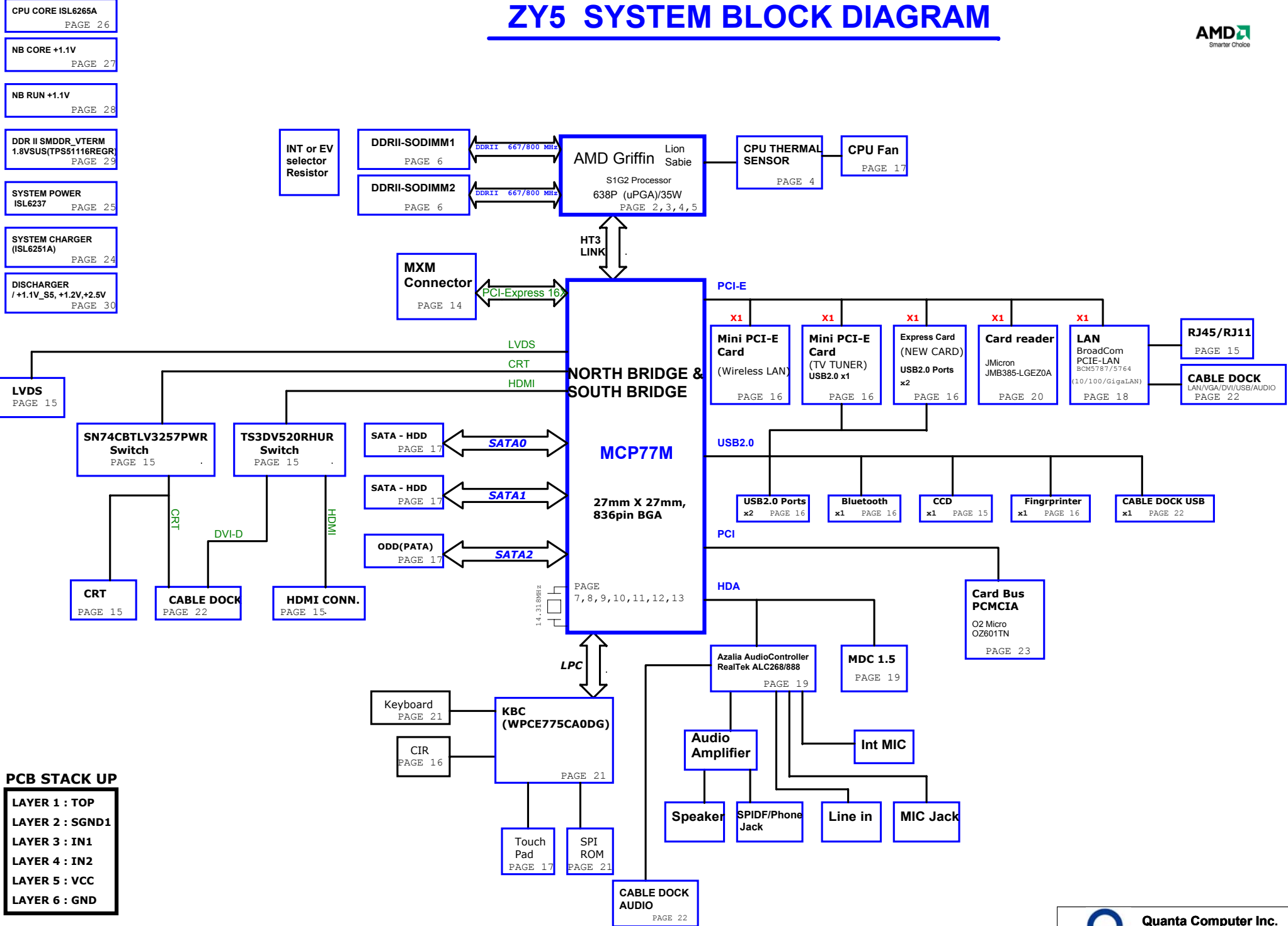


ZY5 SYSTEM BLOCK DIAGRAM



PCB STACK UP

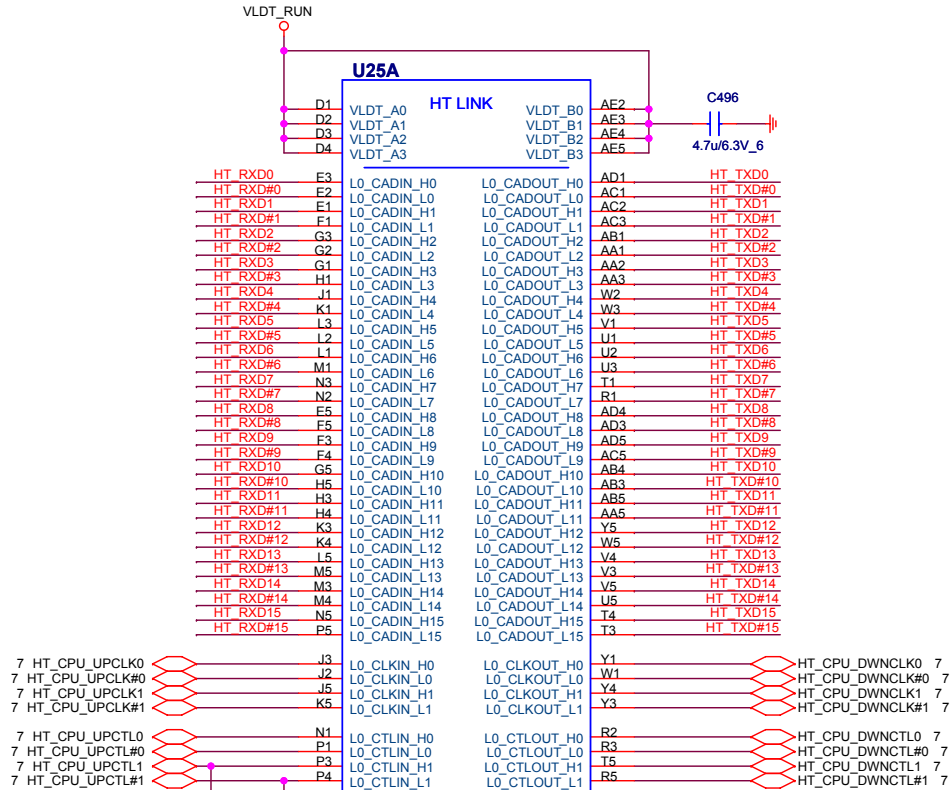
- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : GND



PROCESSOR HYPERTRANSPORT INTERFACE

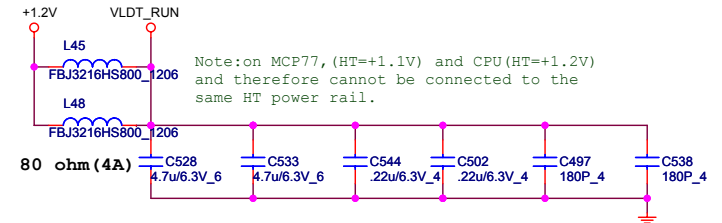
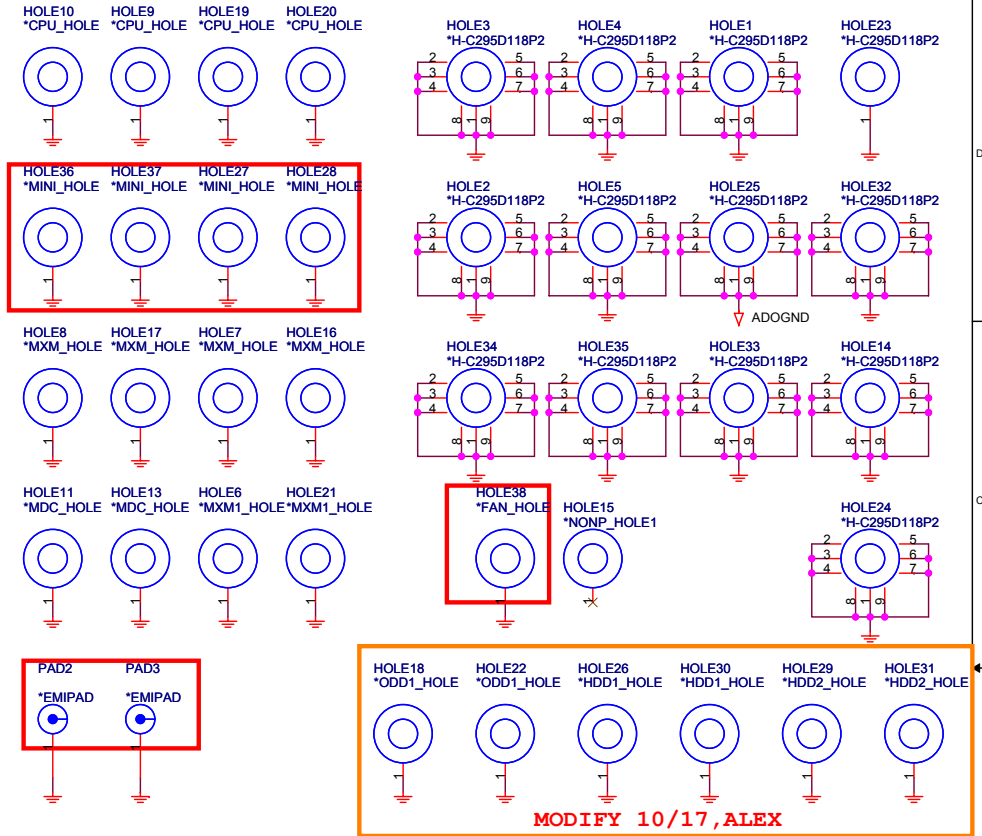
VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

REV:B Modify



NO STUB
for HT3

Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



LAYOUT: Place bypass cap on topside of board



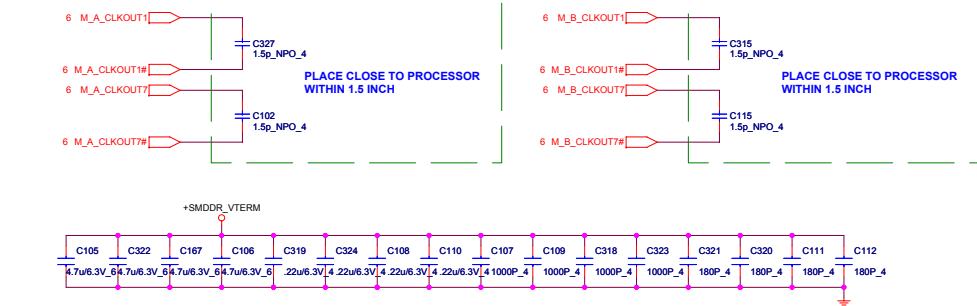
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS



Quanta Computer Inc.

PROJECT : ZY5

Size	Document Number	Rev
		3B
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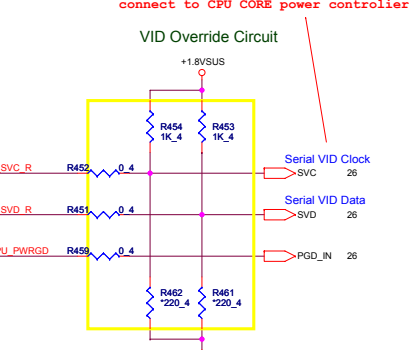
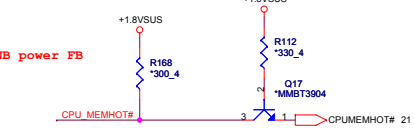
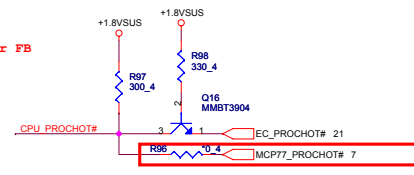
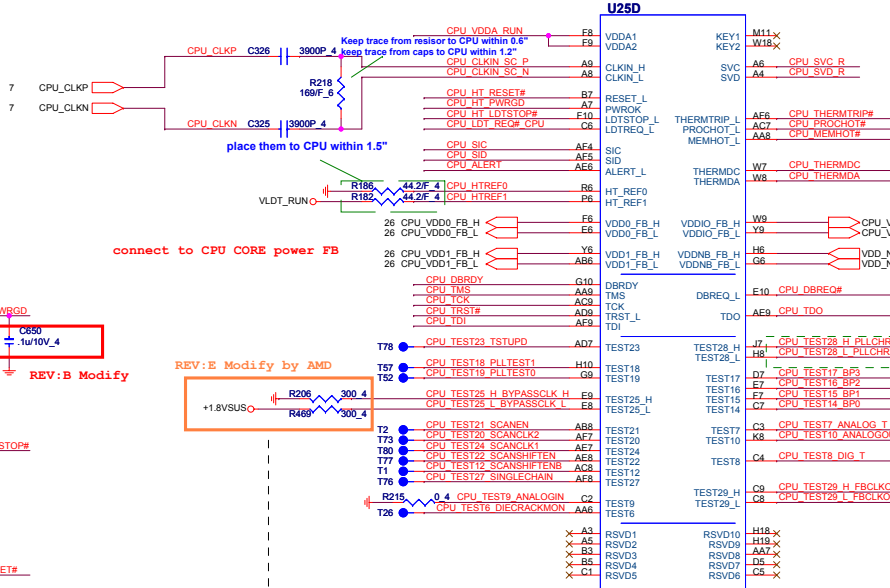
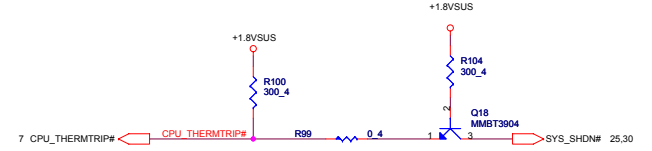
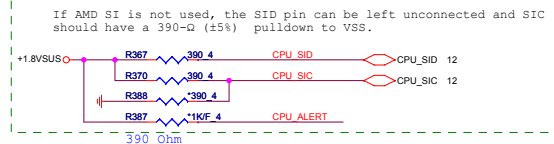
To reverse SODIMM socket



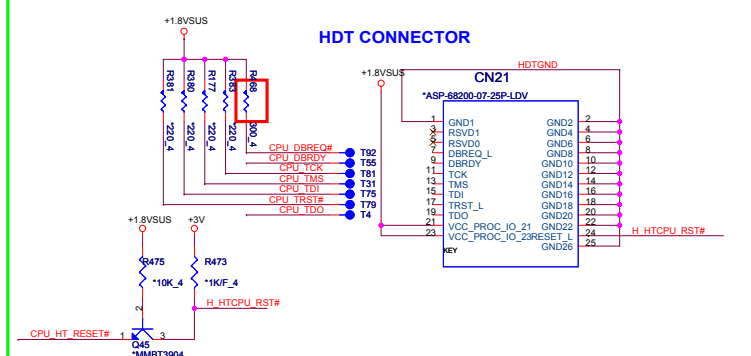
LAYOUT: ROUTE VDDA TRACE APPROX. 60 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

The diagram illustrates the power plane layout for the CPU_VDDA_RUN. It features a +2.5V input connected to a series of components: a capacitor C595 (100u6.3V_3528), an inductor L51 (BLM18P3300SMD_6), and a capacitor C588 (4.7u6.3V_6). This is followed by a capacitor C275 (22u6.3V) and a large capacitor C286 (43300u6.3V). The output is labeled CPU_VDDA_RUN and 3300u6.3V.



VFIX MODE		
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



12/20/08' Reserve 0 ohm for CPU thermal issue on C-test

15 MIL

Address 98H

U7 G786

VCC 1 2 3 4 6 7 8 9

DXN -ALT 1

SMCLK 2

SMCLK 3

DXP 4

-OVT 6

GND 7

+3V

R151 47F_6

R515 0.4

C129 1u10V_4

C117 2200P_4

R136 10K_4

R140 4.7K_4

R143 4.7K_4

R128 10K_4

Q37 2N7002E

Q36 2N7002E

Q35 2N7002E

Q33 2N7002E

To SB GPIO

THERM_ALERT# 12

To FAN

CPUFAN_ON 17

2ND_MBDATA 21

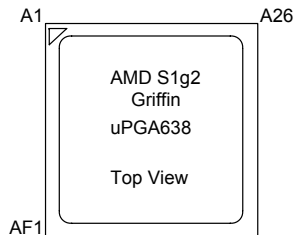
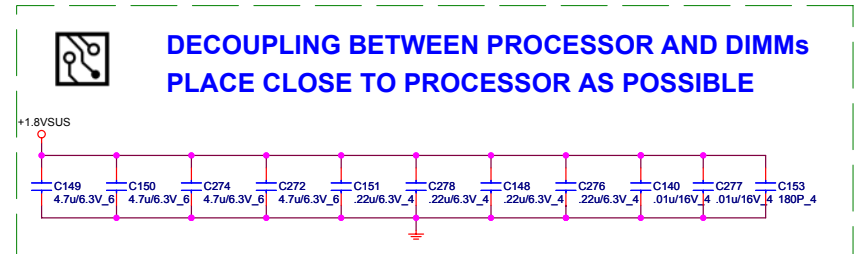
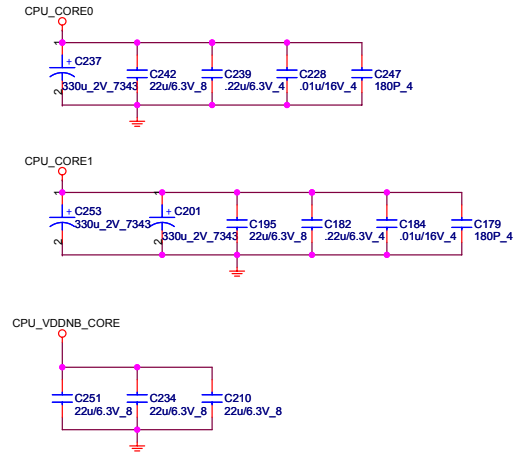
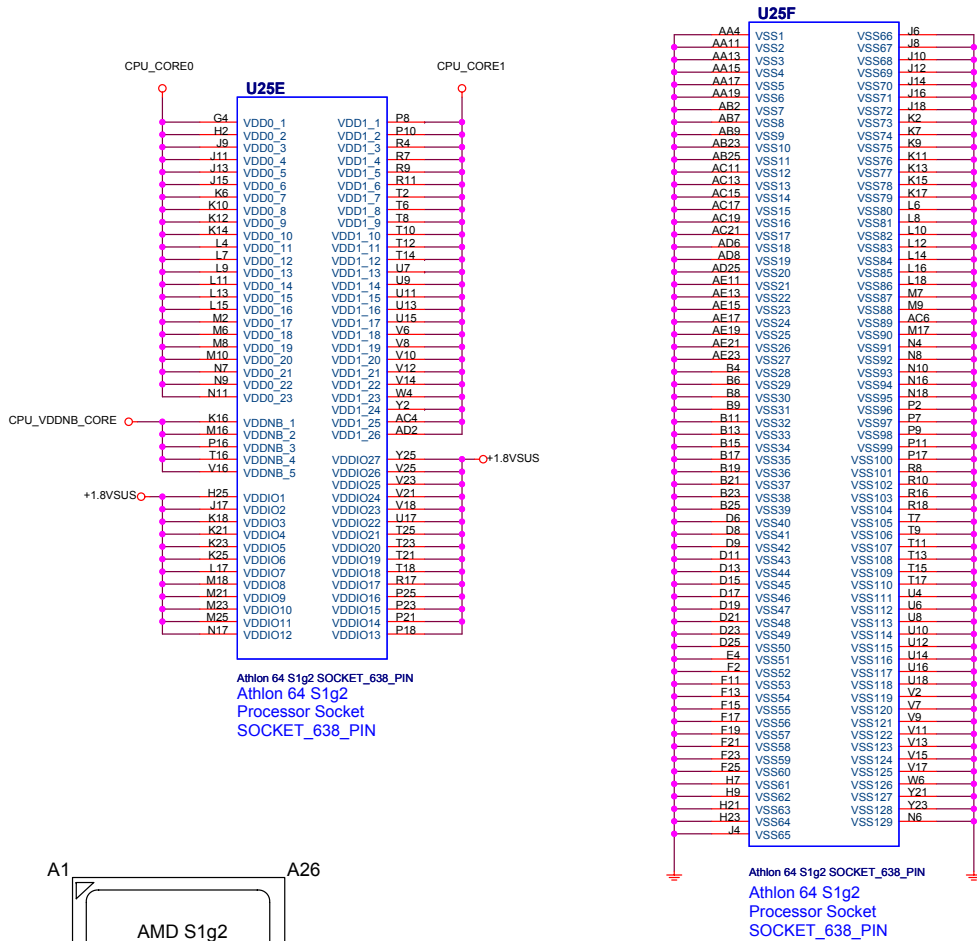
2ND_MBCLK 21

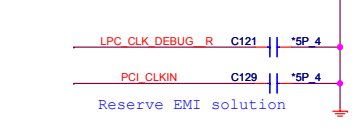
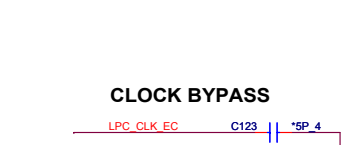
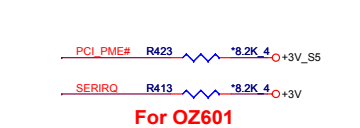
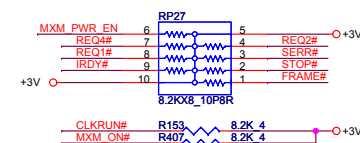
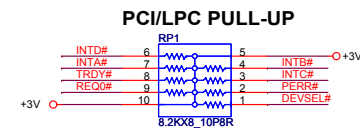
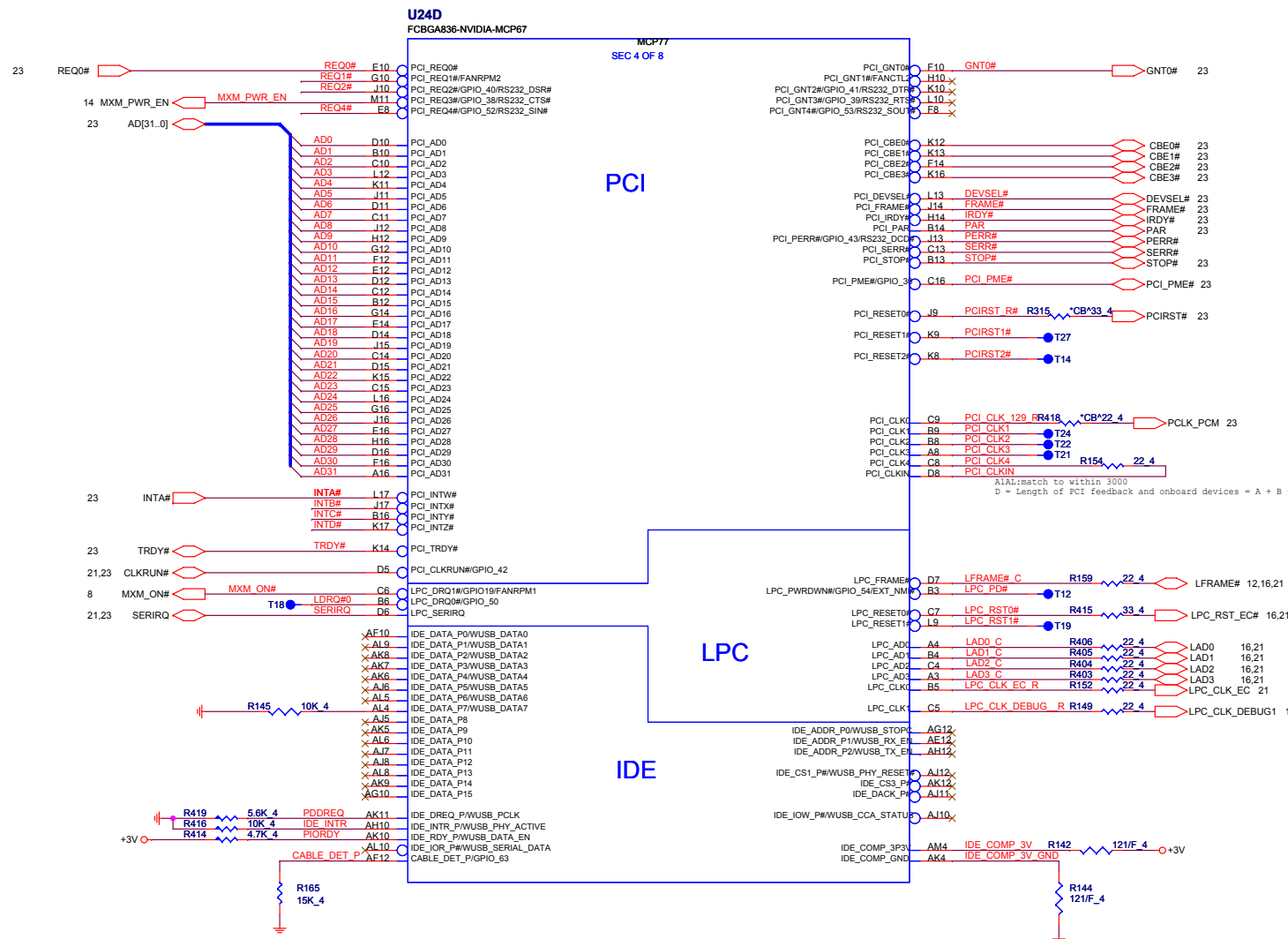
CPU_THERMDC

CPU_THERMDA

10 mil trace / 10 mil space

PROCESSOR POWER AND GROUND





U24C
FCBGA836-NVIDIA-MCP67

LAN

DACS

**FLAT
PANEL**

56mA
24mA

133mA

[LVDS]

133mA

12mA

300mA

110mA

60mA

6mA

63mA

300mA

110mA

60mA

300mA

110mA

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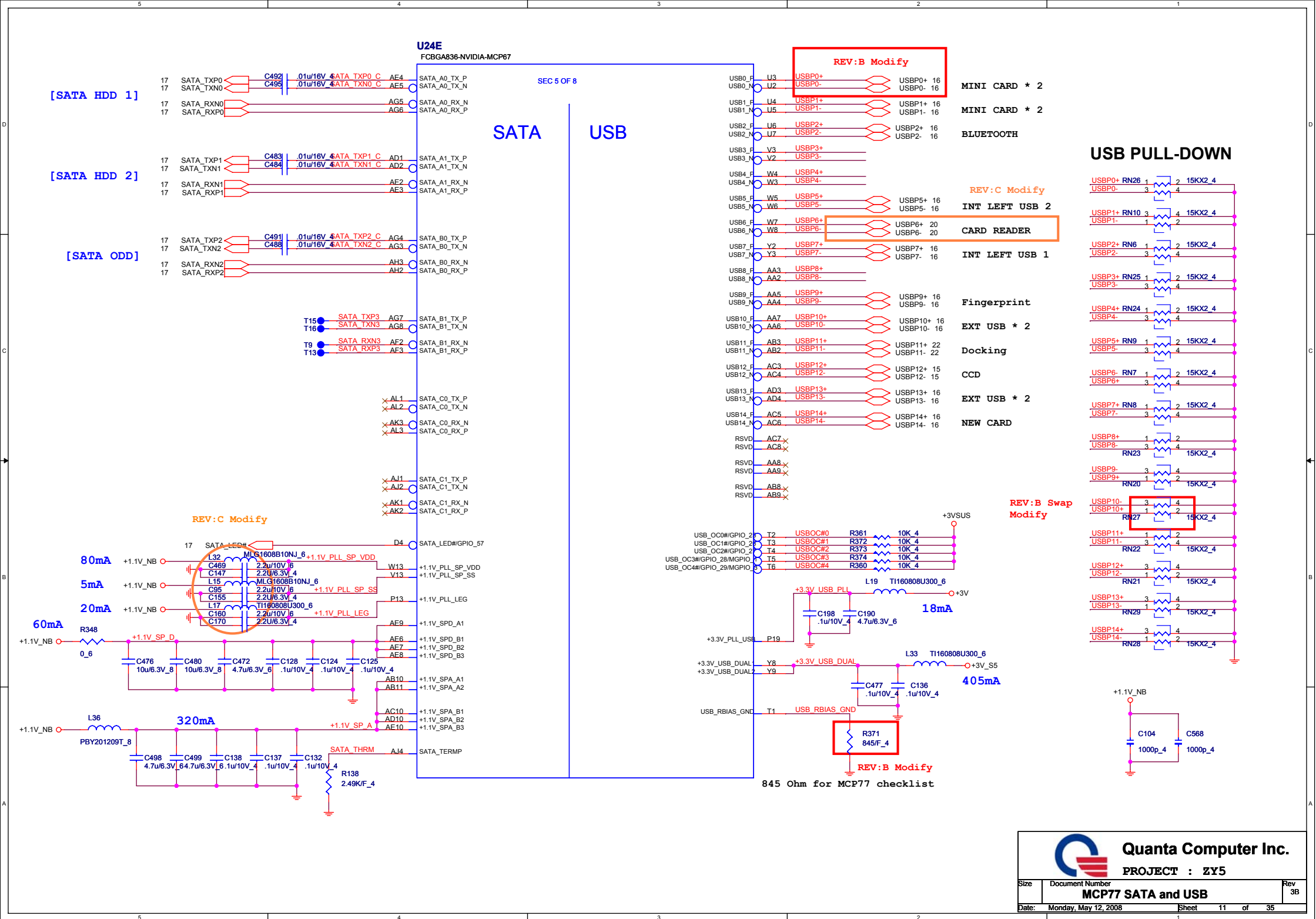
60mA

300mA

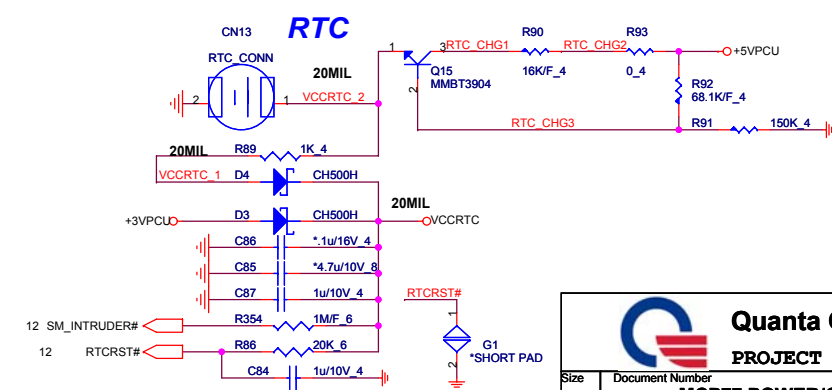
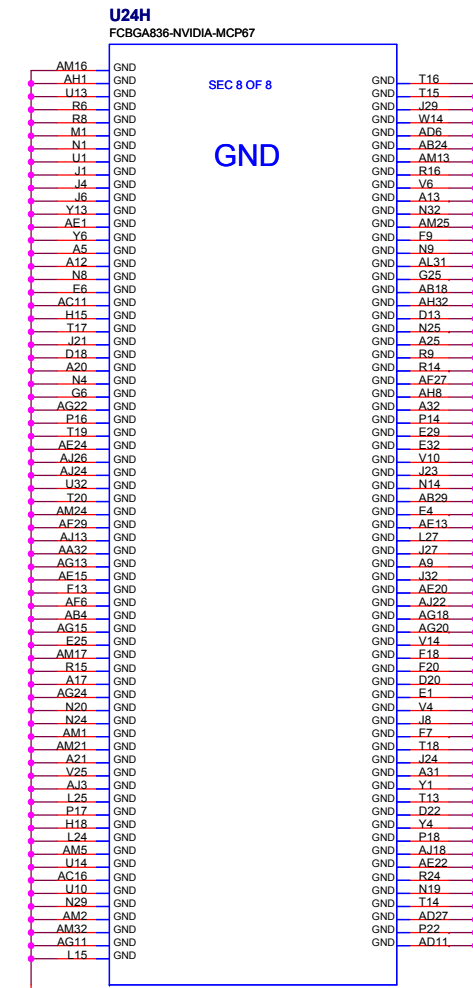
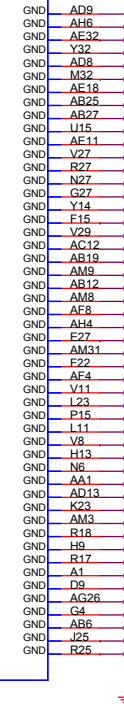
110mA

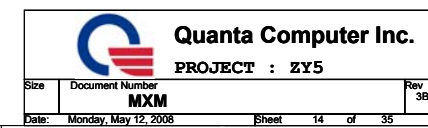
60mA

300mA

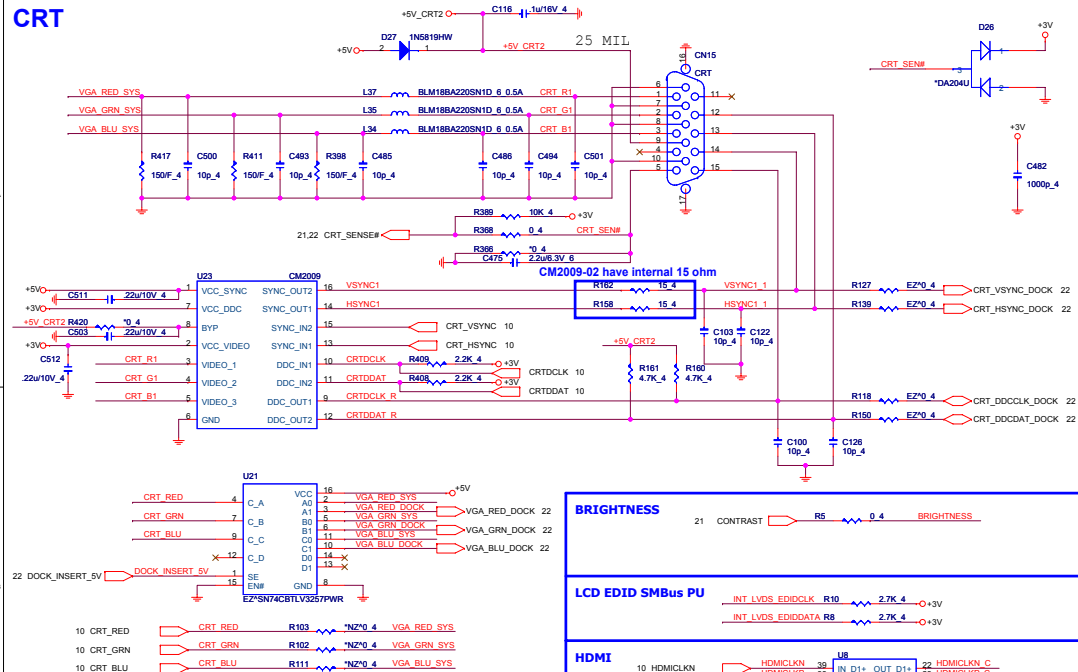


change footprint from 0603 to 0805

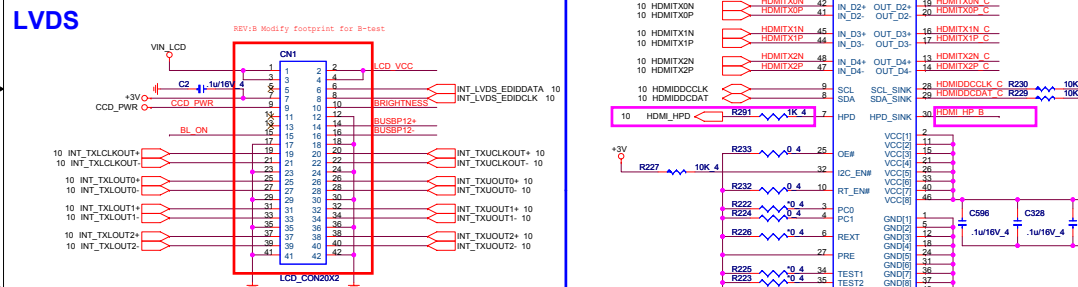




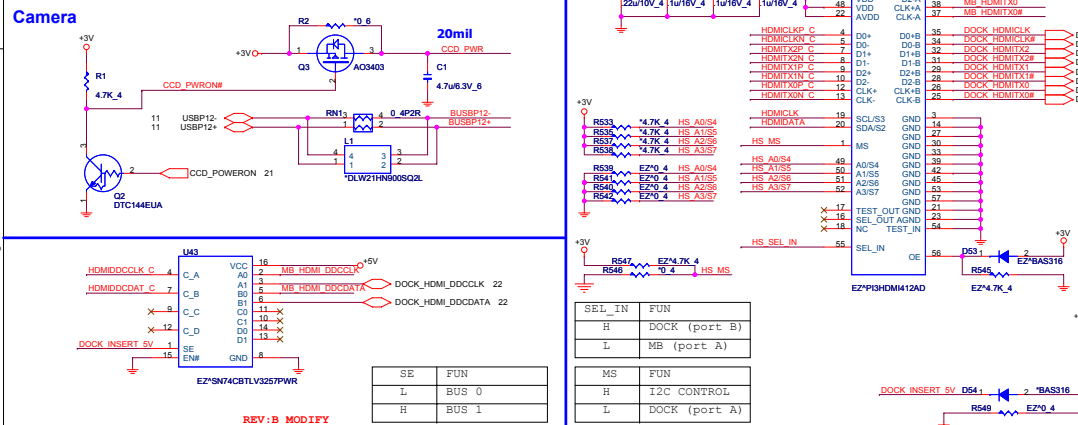
CRT



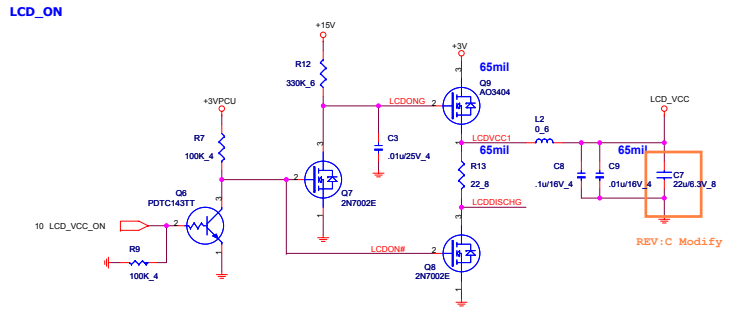
LVDS



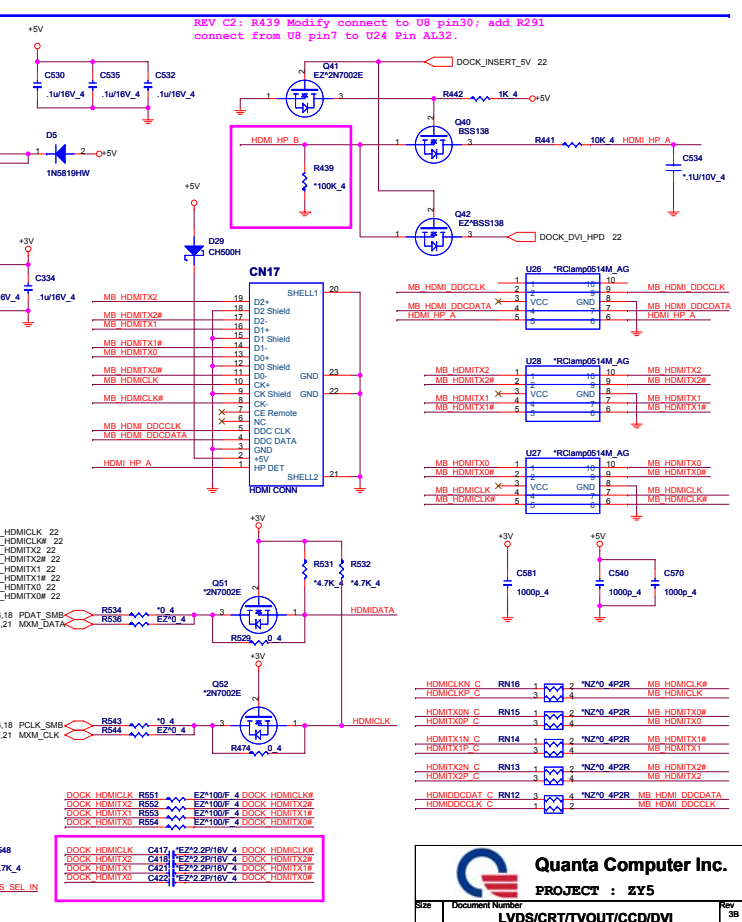
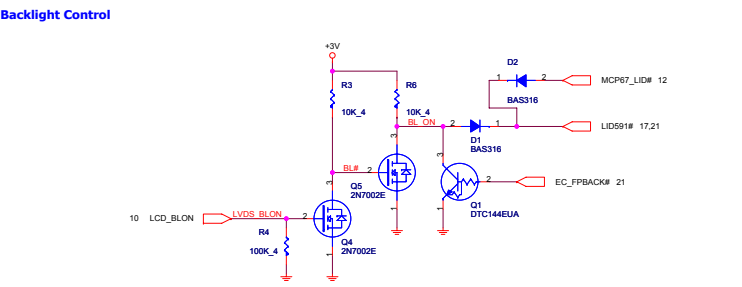
Camera



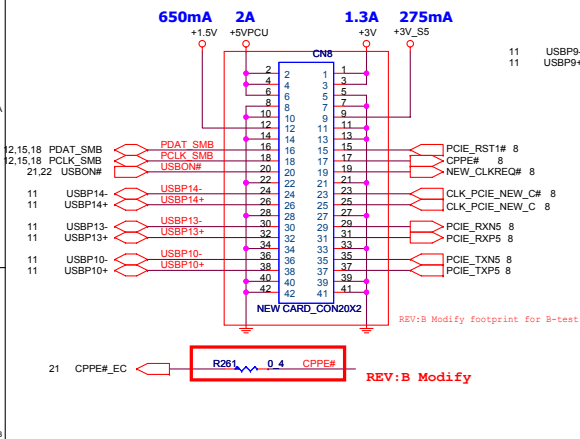
LCD_ON



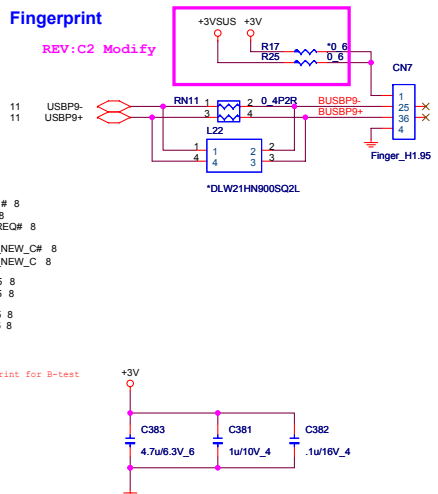
Backlight Control



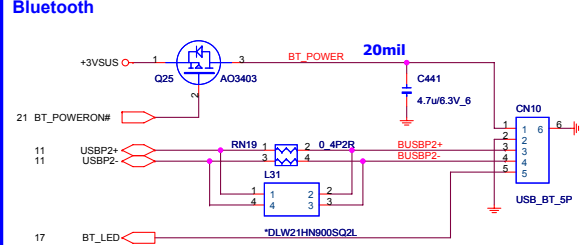
To NEW-CARD & EXT. USB



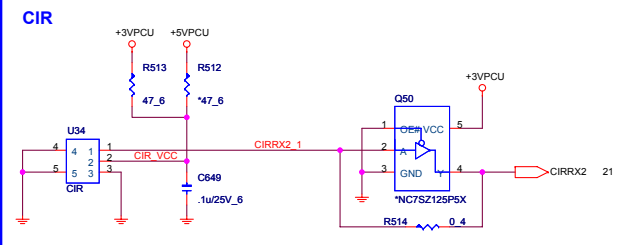
Fingerprint



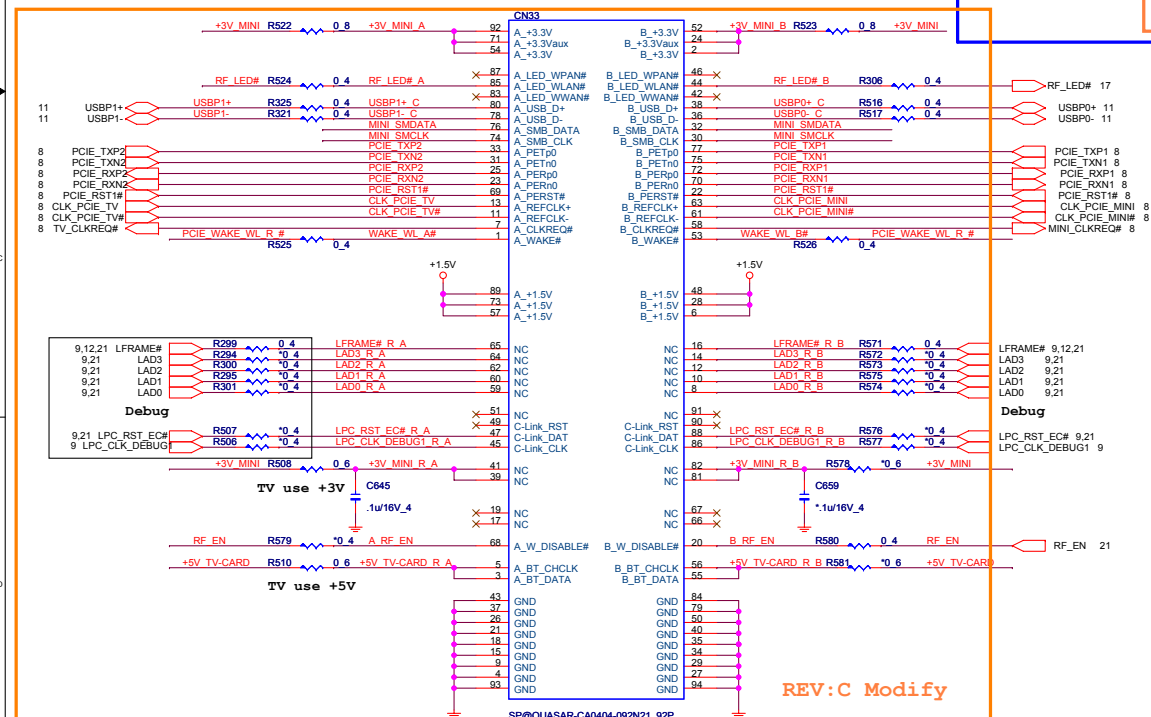
Bluetooth



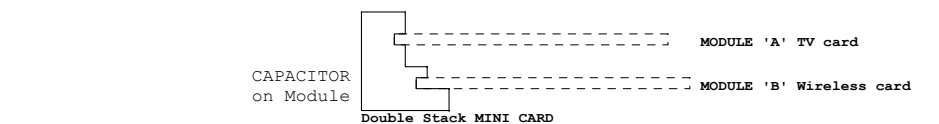
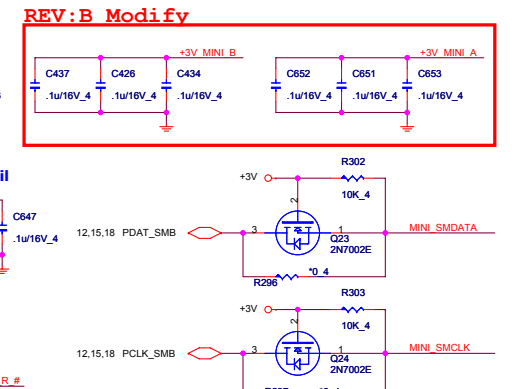
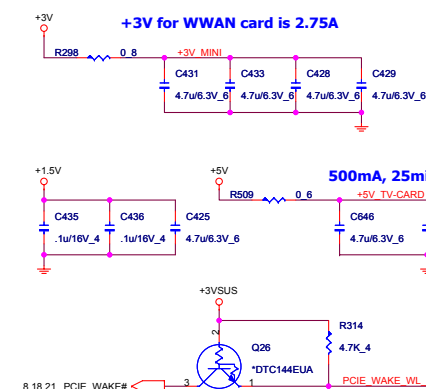
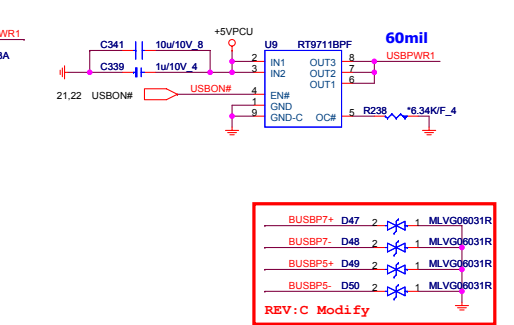
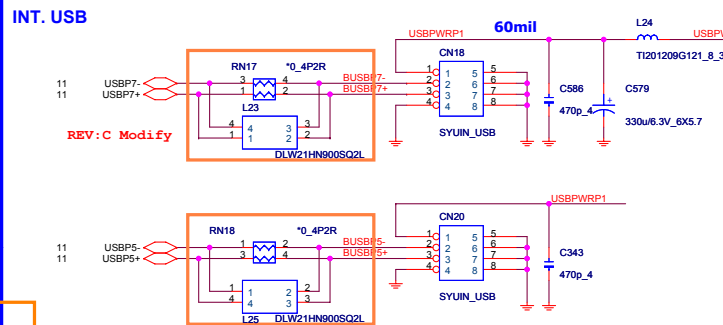
CIR



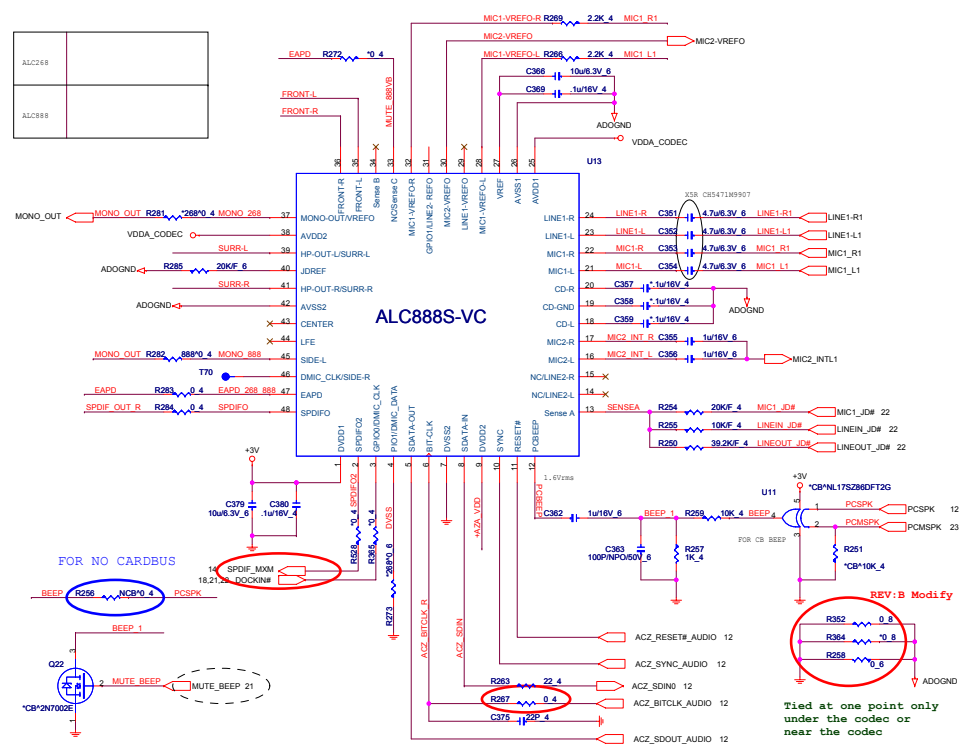
MINI-CARD



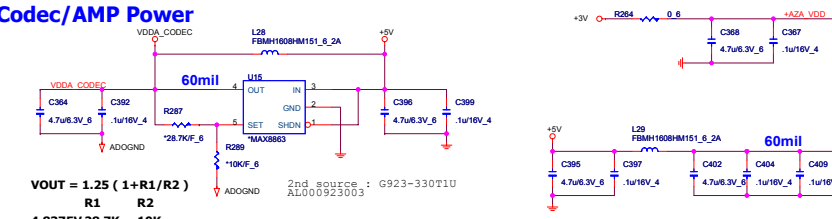
INT. USB



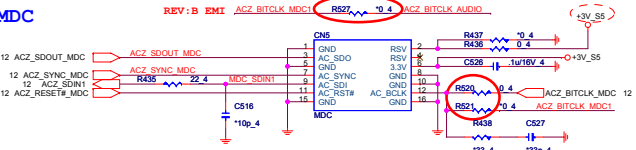
CODEC



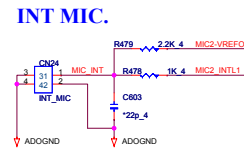
Codec/AMP Power



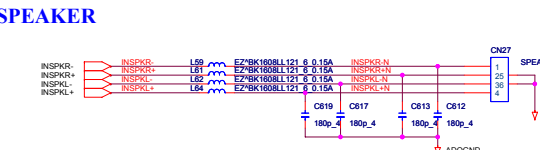
MDC



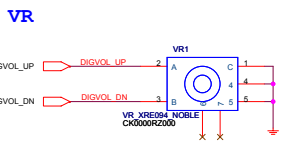
INT MIC.



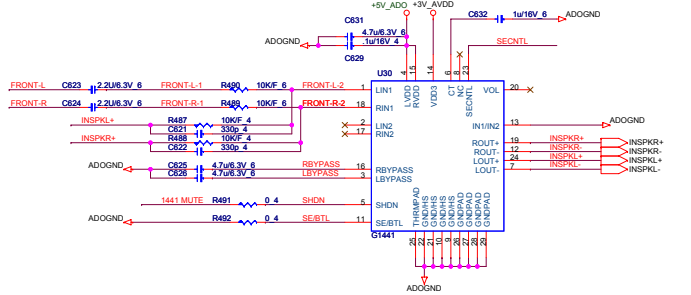
SPEAKER



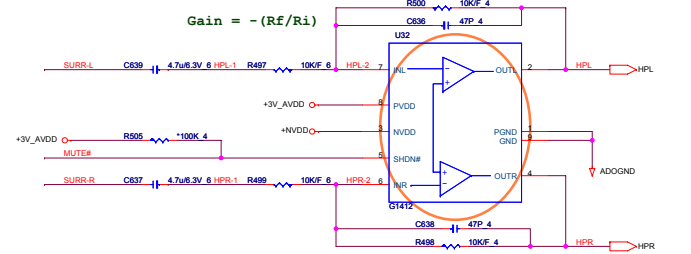
VR



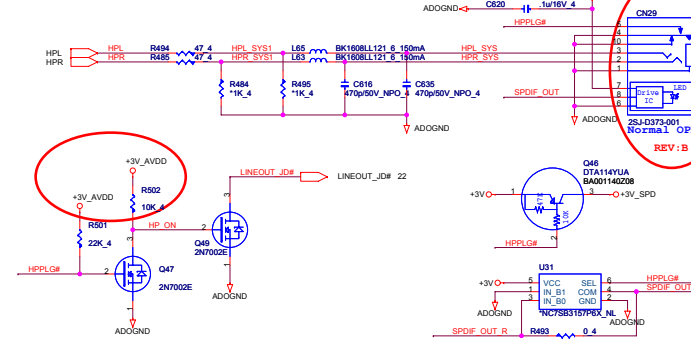
Speaker Amplifier



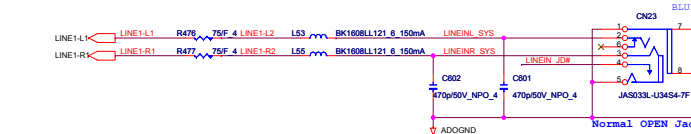
LINE OUT Amplifier



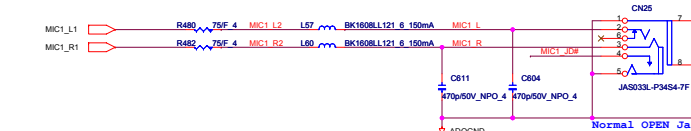
LINE OUT/SPDIF



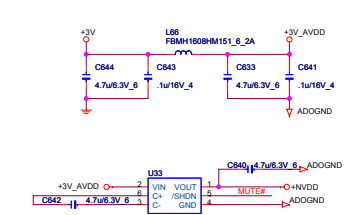
LINE IN



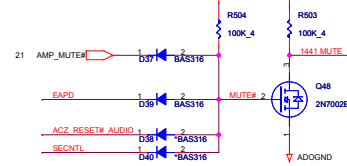
MIC



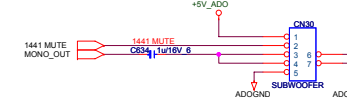
Amplifier POWER



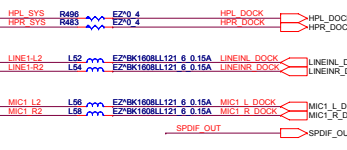
MUTE



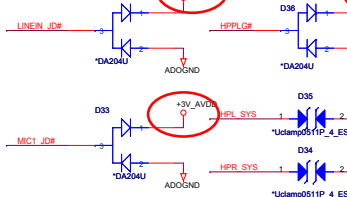
SUBWOOFER



TO DOCKING

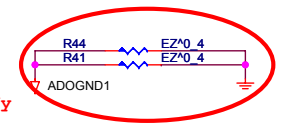
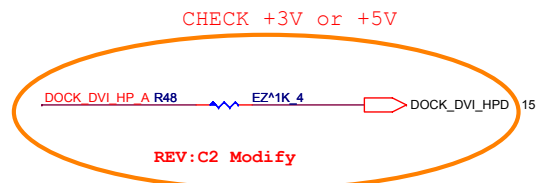
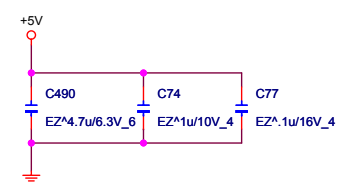
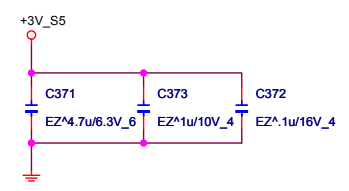
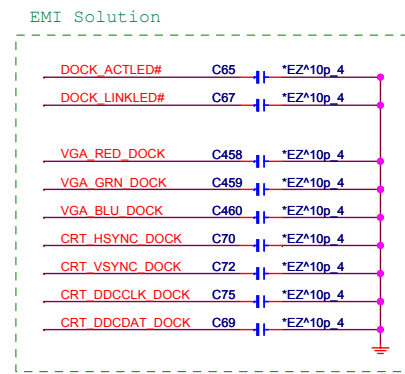
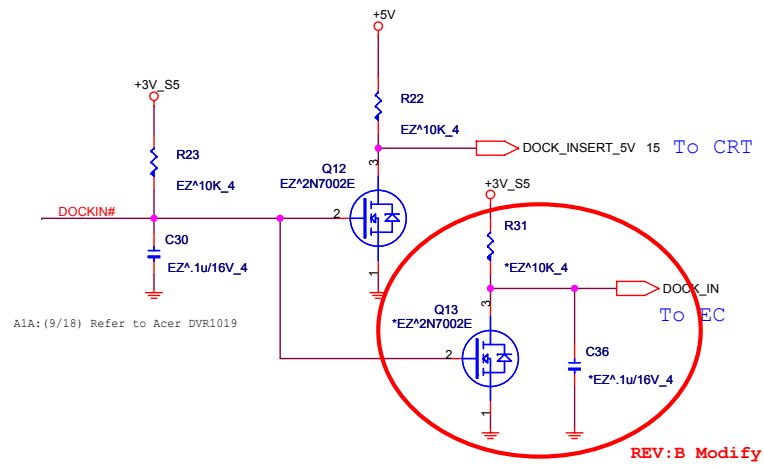
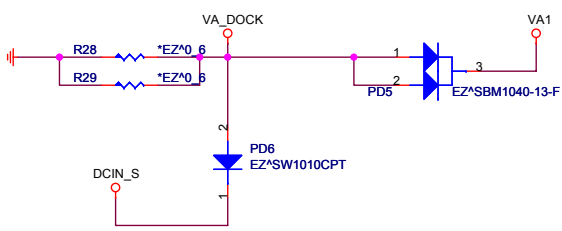
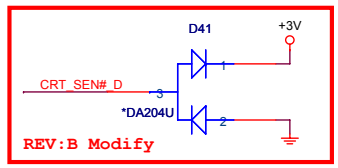
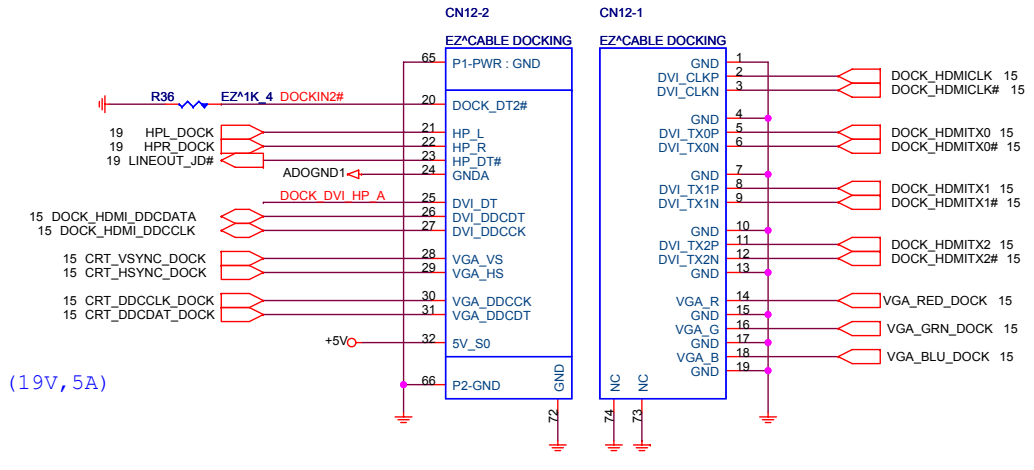
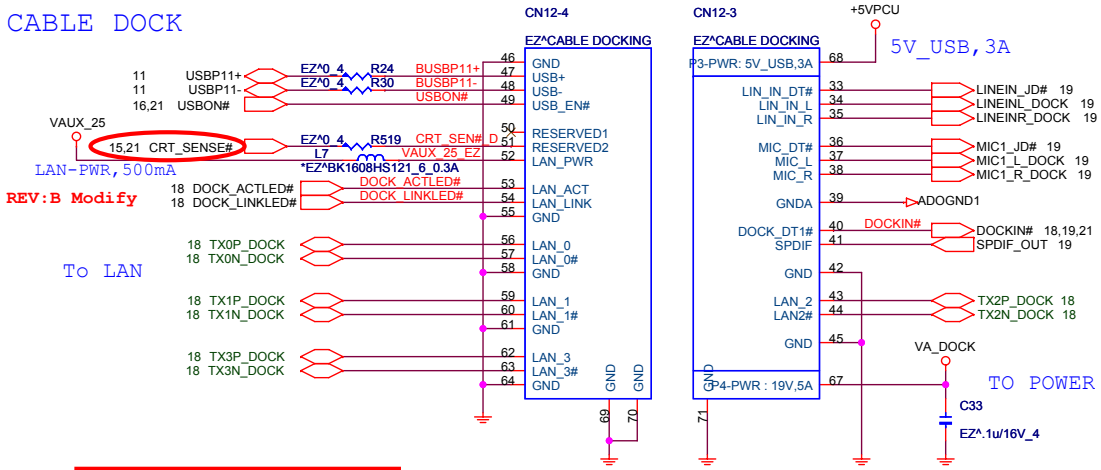


ESD



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CABLE DOCK



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CABLE DOCK

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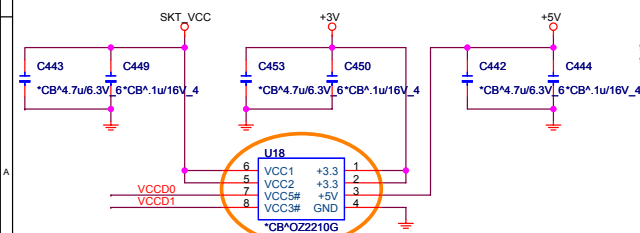
THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP PGM TO CREATE VPP VCC.

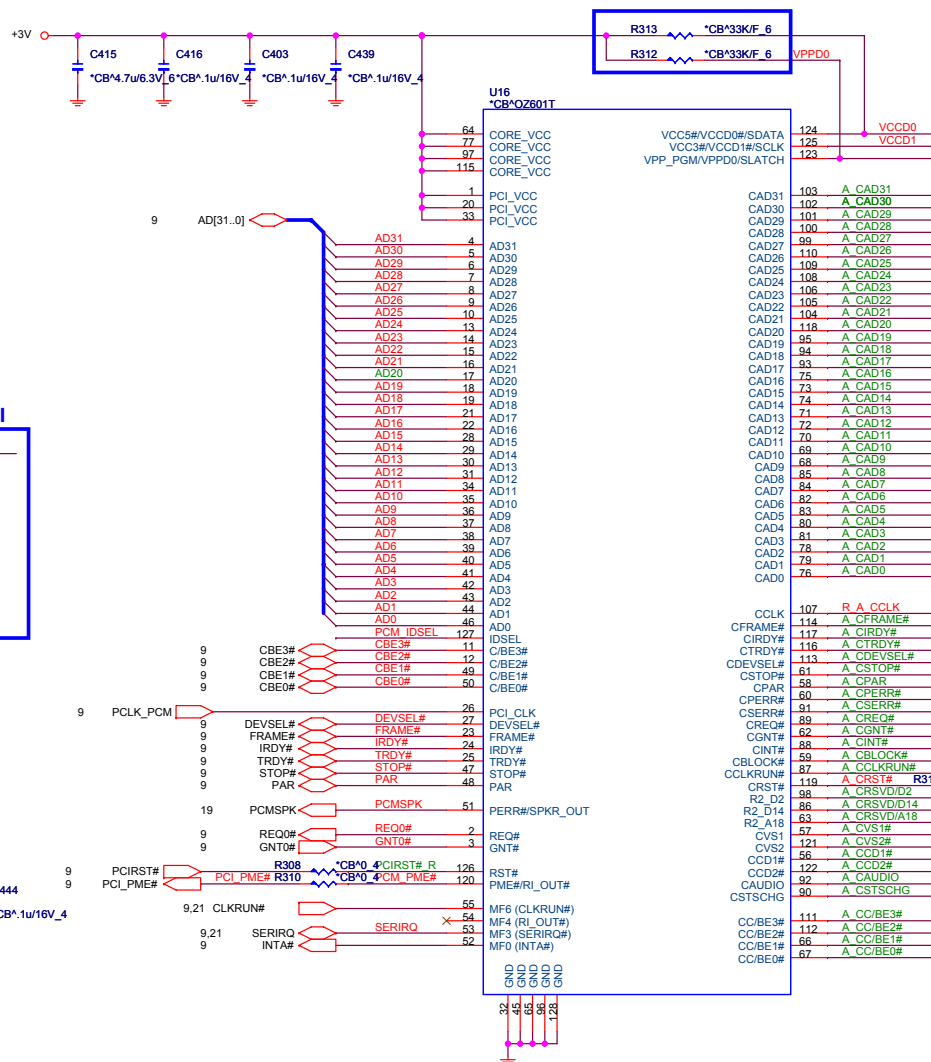
VCC5# (124)	VFP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

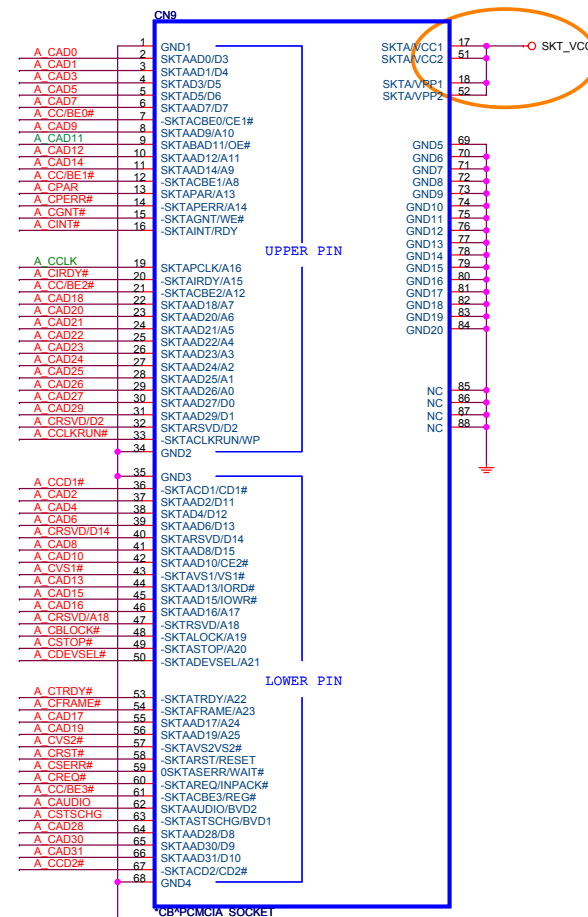


Check Footprint & P/N

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

Check it

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PCMCIA(OZ601)

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REV:B for EMI

REV:B Change foot print

REV:B Del

REV:B Add

REV:B Change source

REV:B for EMI

REV:E Change

REV:B Change foot print

REV:B Change

REV:B Modify

REV:B for EMI

REV:B Change

Input sense resistor and Constant power setting table

	65W UMA	90W MXM
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

REV:B Add only for Acer

$LIM = (1/R1) * (((0.05/VREF=2.39) VACLIM) + 0.050)$
 $CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$
 $4.026A = (1/0.02) * ((0.05/2.365) VACLIM + 0.05)$
 $VACLIM = ((R3//154) / (R2//152 + R3//152)) * Vref$
 $R1 = \text{adapter current sense resistence}$

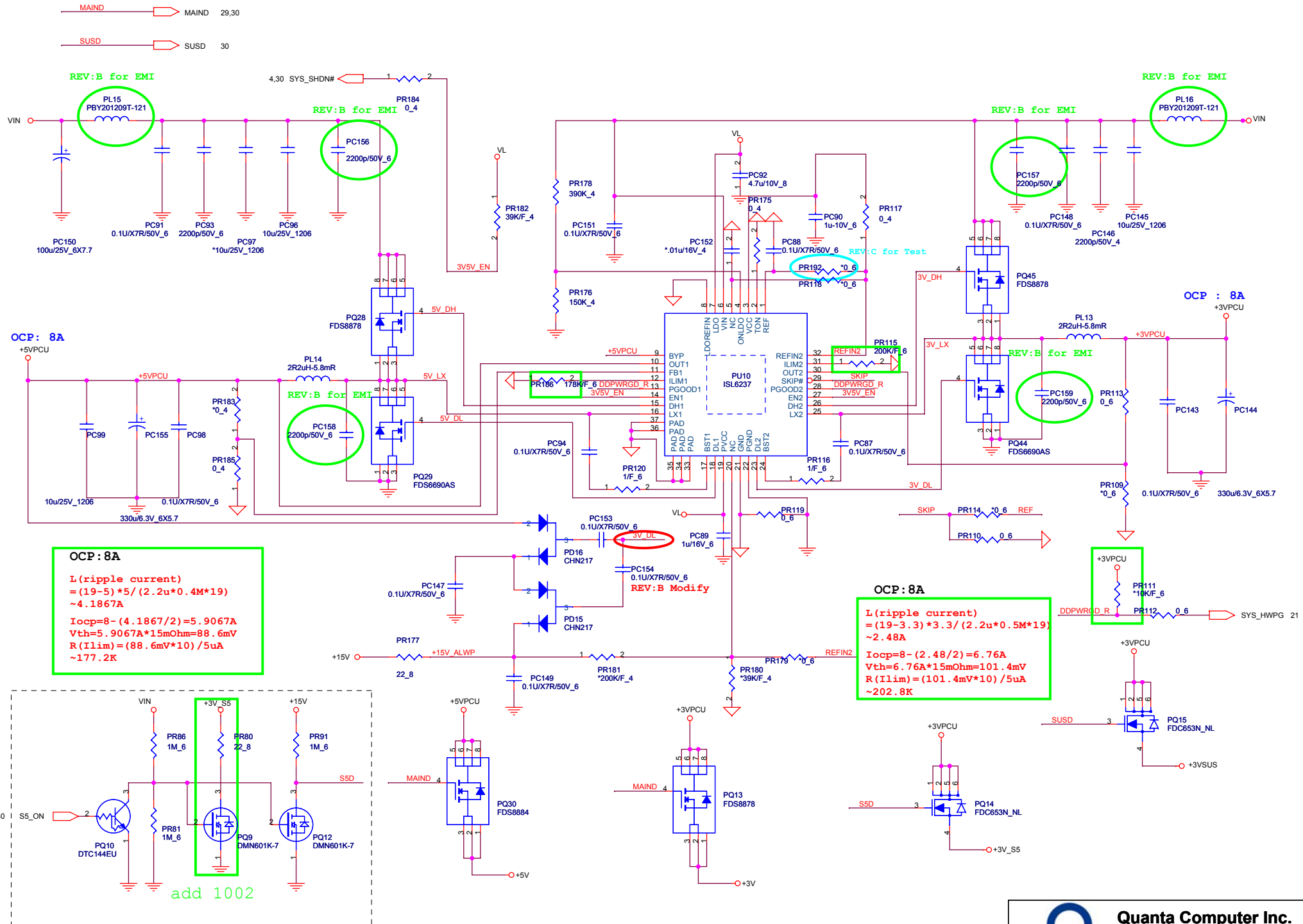
CELL-SET = Hi ----> Cells = VDD ---->4S
 CELL-SET = Low ----> Cells = GND ---->3S

A: (9/7) Add ESD diode base on EC FAE suggestion



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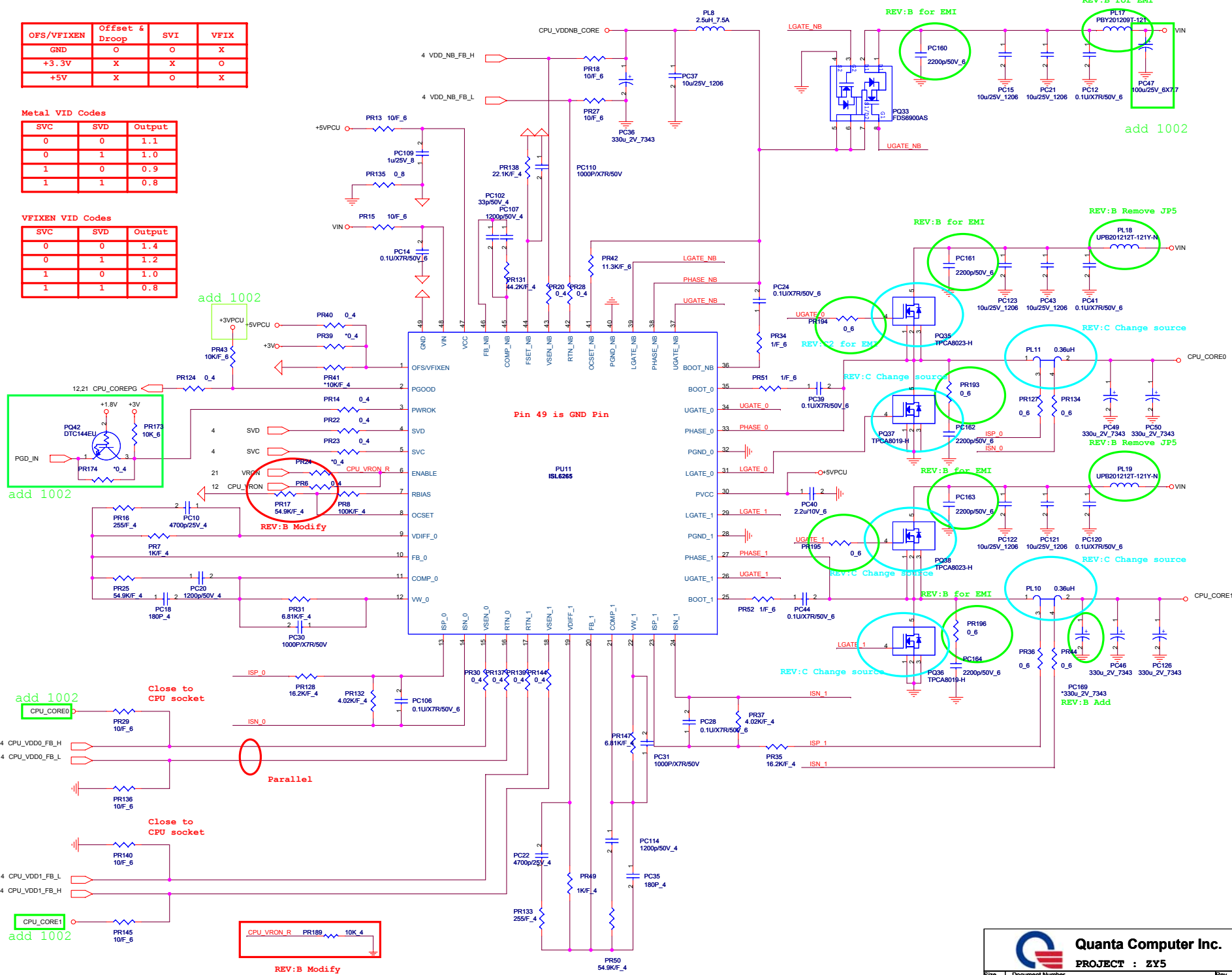
Size	Document Number	Rev
	CHARGER (ISL6251A)	3B
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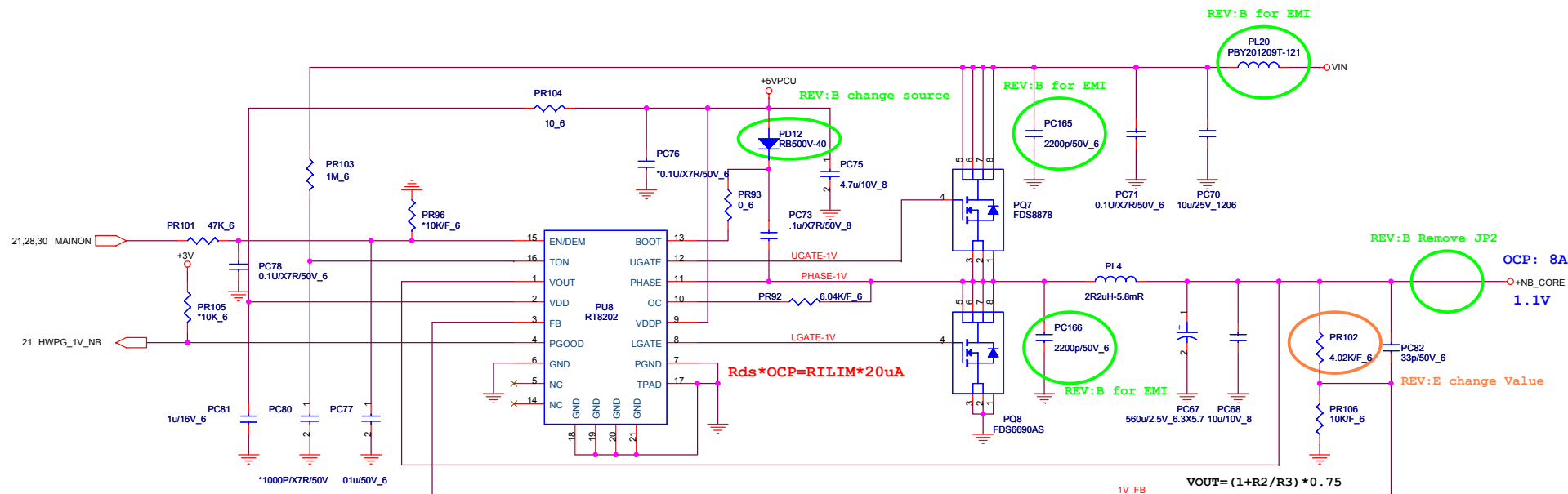


OFS/VFIXN	Offset & Droop	SVC	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

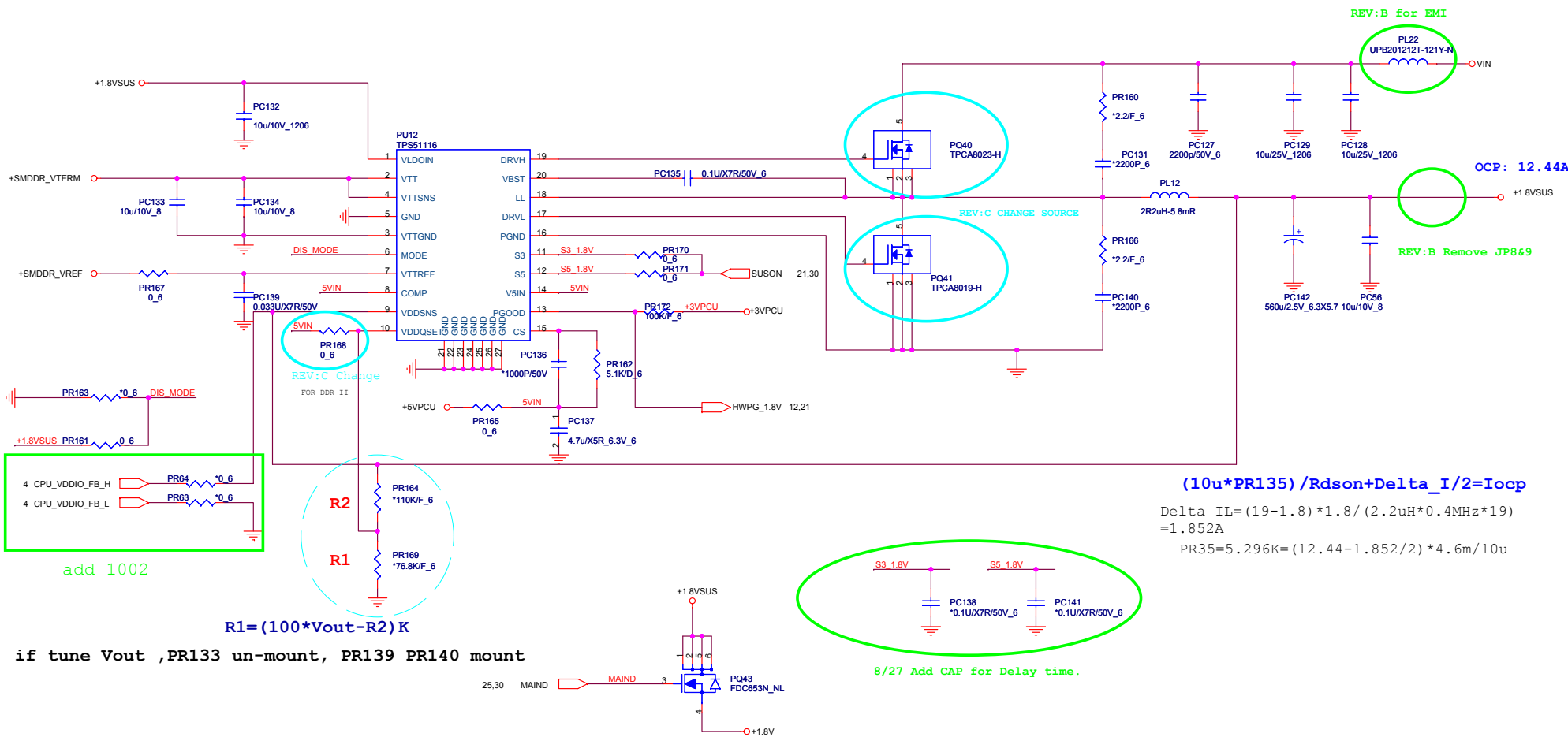




$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

8A OCP --- OC=6.04K
FDS6690AS Rds=15mOhm

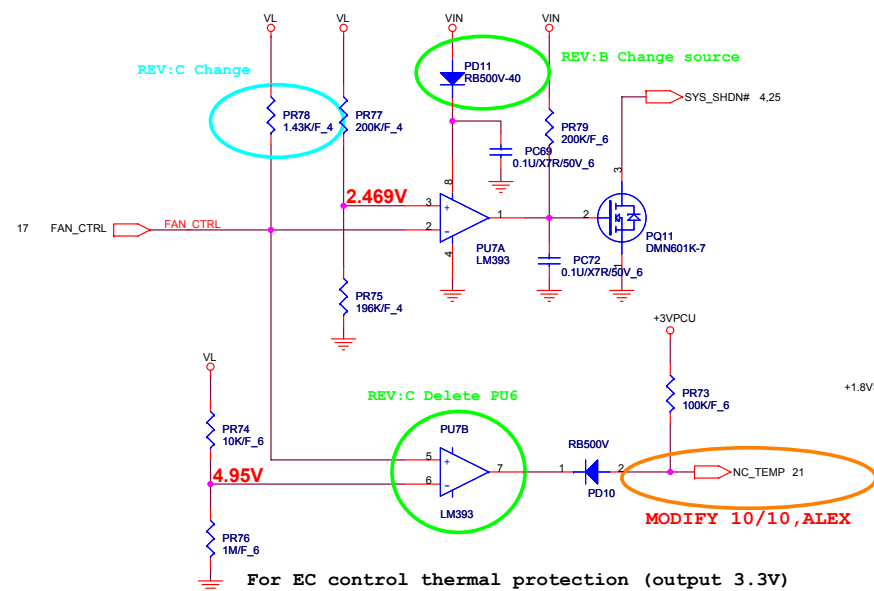


$$(10u \cdot PR135) / R_{dson} + \Delta I / 2 = I_{ocp}$$

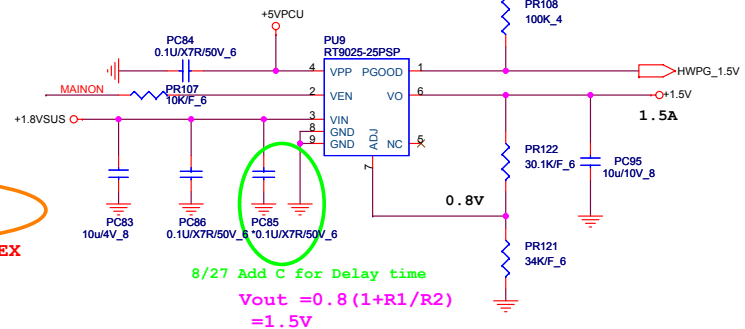
$$\Delta I_L = (19 - 1.8) \cdot 1.8 / (2.2uH \cdot 0.4MHz \cdot 19) = 1.852A$$

$$PR35 = 5.296K = (12.44 - 1.852 / 2) \cdot 4.6m / 10u$$

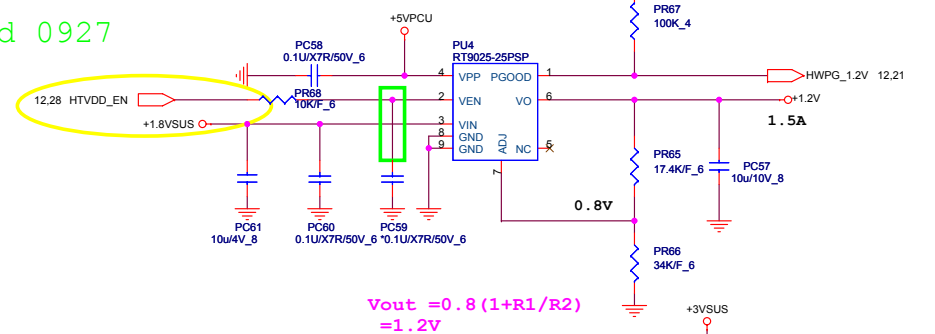
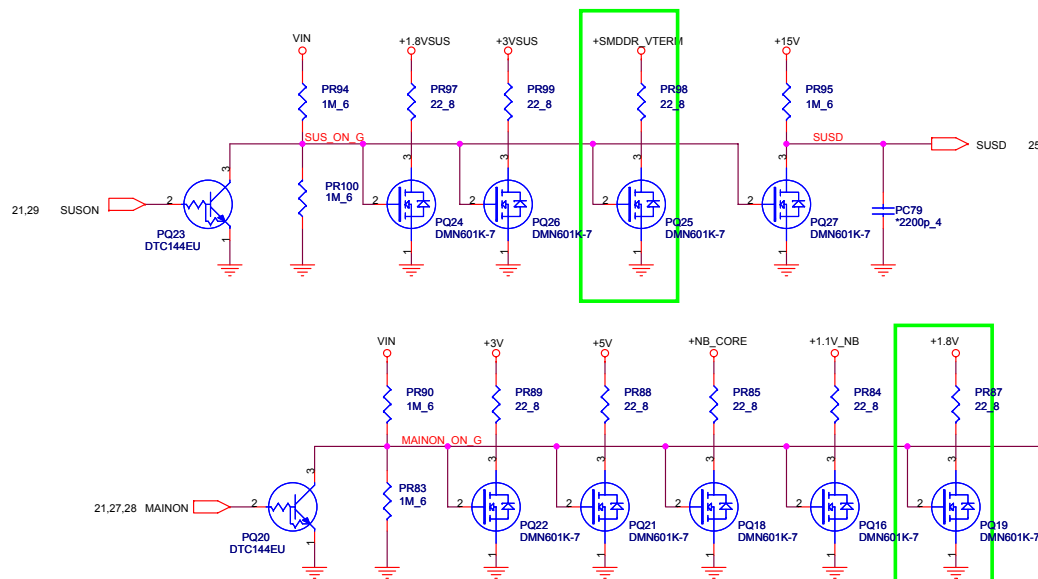
NTC resistor on Thermal module



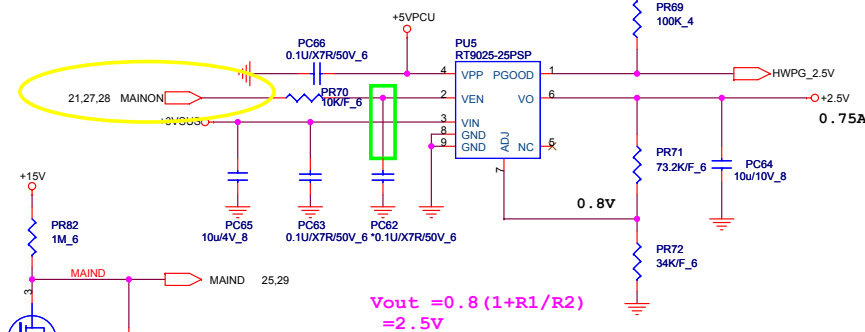
```
add 0927
```



```
add 0927
```

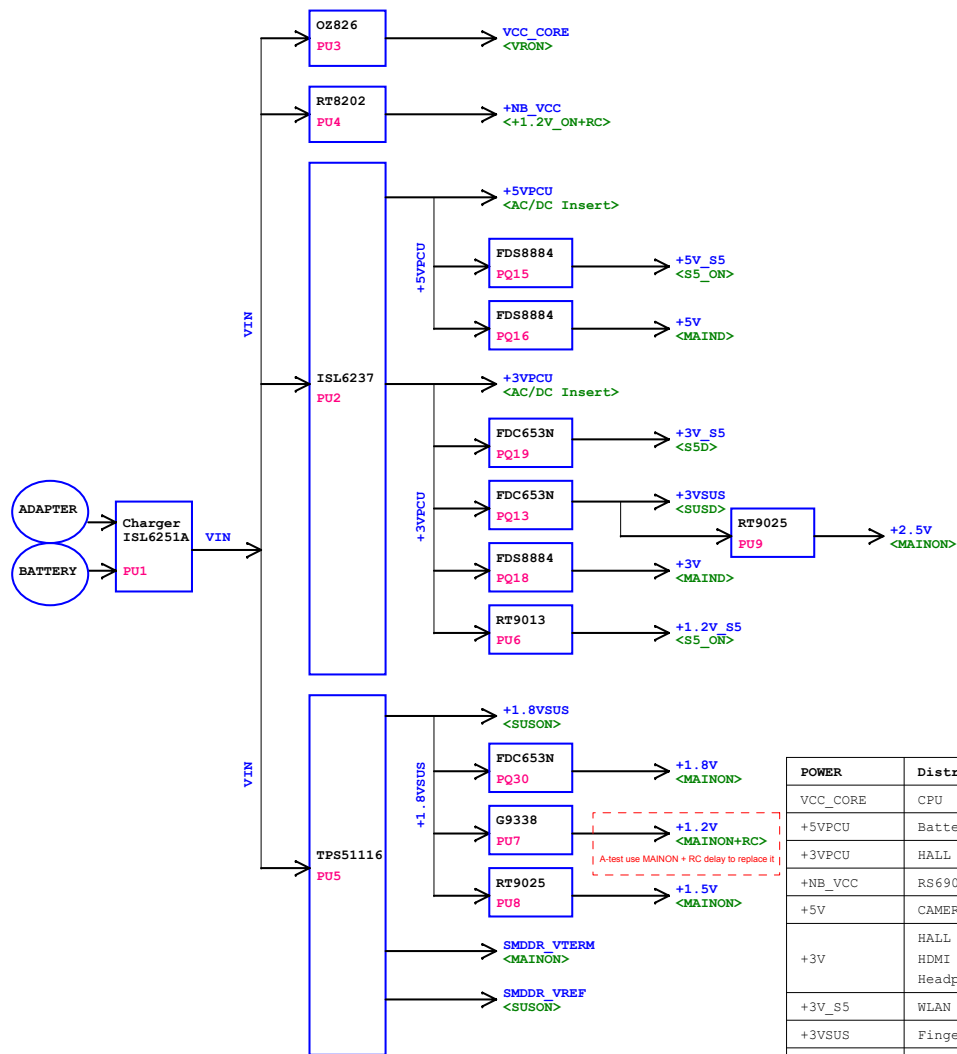

$$V_{out} = 0.8(1 + R_1/R_2) = 1.2V$$


```
add 1002
```

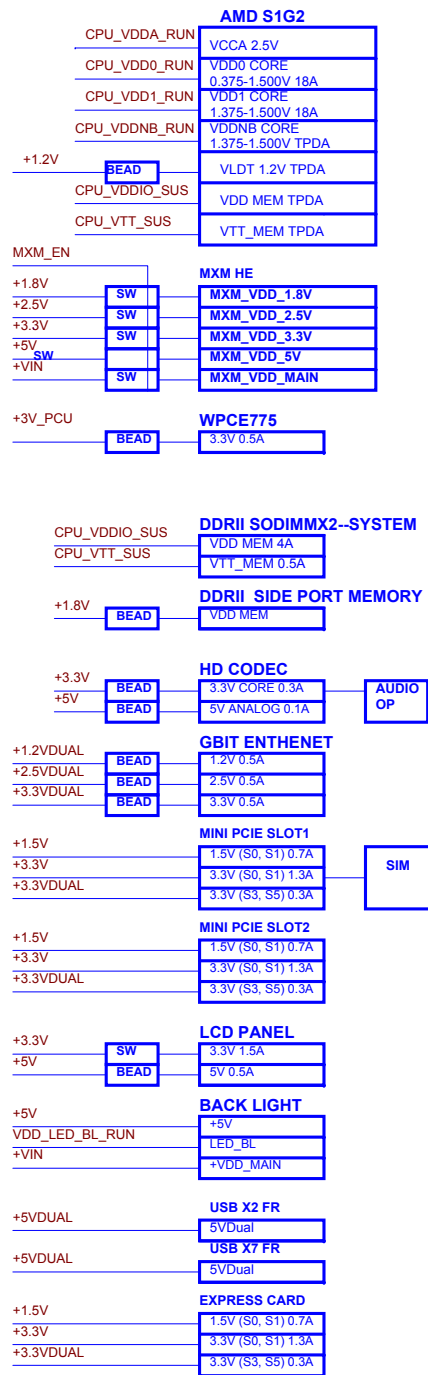

$$V_{out} = 0.8 (1 + R_1/R_2) = 2.5V$$
**Quanta Computer Inc.**

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	Discharge (1.1V/1.2V/2.5V)	3E
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POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	



ZY5 Power on Sequence

